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EXAMINER	
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2618	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)
	10/673,263	SHIRVANI ET AL.
	Examiner	Art Unit
	Adeel Haroon	2618

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-125* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-30* is/are allowed.

6)☒ Claim(s) *31-125* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/6/06 has been entered.

Response to Arguments

2. Applicant's arguments filed 11/6/06 with respect to claims 31, 51, 71, 90, 101, and 117 have been fully considered but they are not persuasive.

The applicant argues that Pollanen fails to disclose the amended limitation of measuring at least one of an output voltage and an output current of an antenna of the transmitter. The examiner respectfully disagrees. Pollanen teaches that voltage and current are measured via transistor T1 (Column 4, lines 14-37) and further teaches that this "load impedance preferably comprises an antenna" (Column 6, lines 56-60).

Thereby, Pollanen measures at least one of an output voltage and output current of antenna of the transmitter.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 31-39, 41, 45-49, 51-59, 61, 65-69, 71-79, 81, 85-88, 90-96, 101-107, 111-115, and 117-122 are rejected under 35 U.S.C. 102(b) as being anticipated by Pollanen et al. (U.S. 6,289,205).

With respect to claim 31, Pollanen et al. disclose a system for controlling true output power of a transmitter in figure 9. Pollanen et al. disclose a voltage detector in communication with a power amplifier, which is in the transmitter element number 3, for detecting an output voltage, Vrf, of the power amplifier, which is proportional to the output voltage of the amplifier(Column 4, lines 14-27). Pollanen et al. also disclose a current detector that generates a current signal, Irf, that is proportional to the output current of the power amplifier (Column 4, lines 28-37). Pollanen et al. disclose a power detector in communication with the voltage detector and the current detector comprising

a multiplier, element number M1, for multiplying the current signal and the voltage signal to generate a power signal, Pwdc, proportional to the true output power delivered by the power amplifier (Column 4, lines 38-47). Pollanen et al. further disclose a power controller, element number 6, in communication with the power detector and power amplifier for controlling the power amplifier to regulate the true output power delivered by the power amplifier based on the power signal (Column 7, lines 39-52 and Column 2, lines 36-42). Pollanen et al. further teach that the output voltage and output current of the power amplifier in element 3 are the output voltage and current of an output load, element number 4, of the transmitter ((Column 6, lines 40-41).

With respect to claim 32, Pollanen et al. disclose that the voltage signal and current signal, Vrf and Irf, must comprise a fundamental frequency component of the output voltage and current of the power amplifier since they are taken from the output stage of the amplifier (Column 4, lines 14-37). Pollanen et al. also disclose that eh power comprise a DC power signal, Pwdc (Column 4, lines 38-47).

With respect to claims 33-35, Pollanen et al. disclose a voltage scaler, comprising a capacitive voltage divider, element numbers C3, T1, and A1, for scaling the output voltage of the power amplifier (Column 4, lines 15-27).

With respect to claims 36 and 37, Pollanen et al. disclose voltage scaling ratio controller, element number A1, which as a result of its operation sets the voltage scaler based upon a predetermined target output power of the amplifier.

With respect to claim 38, Pollanen et al. disclose a current mirror, combination of element numbers T1 and A2, for mirroring the output current wherein the output current is scaled using a predetermined current scaling ratio in A2 (Column 4, lines 28-37).

With respect to claim 39, Pollanen et al. disclose a linear multiplier, M1, in figure 9.

With respect to claim 41, Pollanen et al. teach generating a control signal to vary the true output power delivered by the power amplifier by the control line from element number 6 to element number 3 in figure 9 (Column 7, lines 39-52).

With respect to claims 45 and 46, Pollanen et al. disclose that the power controller, power amplifier, voltage detector, current detector, and power detector are formed on a monolithic substrate (Column 3, lines 10-15).

With respect to claims 47 and 48, Pollanen et al. disclose the power amplifier comprises a power controller, voltage detector, current detector, and power detector (Column 3, lines 10-15).

With respect to claim 49, Pollanen et al. disclose the system comprises a transmitter portion, element number 2, of a transceiver in figure 9 (Column 6, lines 34-39).

With respect to claim 51, Pollanen et al. disclose a system for controlling true output power of a transmitter means in figure 9. Pollanen et al. disclose a voltage detector means in communication with a power amplifier means, which is in the transmitter element number 3, for detecting an output voltage, Vrf, of the power amplifier means, which is proportional to the output voltage of the amplifier means

(Column 4, lines 14-27). Pollanen et al. also disclose a current detector means that generates a current signal, Irf, that is proportional to the output current of the power amplifier means (Column 4, lines 28-37). Pollanen et al. disclose a power detector means in communication with the voltage detector and the current detector comprising a multiplier means, element number M1, for multiplying the current signal and the voltage signal to generate a power signal, Pwdc, proportional to the true output power delivered by the power amplifier means (Column 4, lines 38-47). Pollanen et al. further disclose a power controller means, element number 6, in communication with the power detector means and power amplifier means for controlling the power amplifier means to regulate the true output power delivered by the power amplifier means based on the power signal (Column 7, lines 39-52 and Column 2, lines 36-42). Pollanen et al. further teach that the output voltage and output current of the power amplifier in element 3 are the output voltage and current of an output load, element number 4, of the transmitter ((Column 6, lines 40-41).

With respect to claim 52, Pollanen et al. disclose that the voltage signal and current signal, Vrf and Irf, must comprise a fundamental frequency component of the output voltage and current of the power amplifier since they are taken from the output stage of the amplifier (Column 4, lines 14-37). Pollanen et al. also disclose that eh power comprise a DC power signal, Pwdc (Column 4, lines 38-47).

With respect to claims 53-55, Pollanen et al. disclose a voltage scaler means, comprising a capacitive voltage divider means, element numbers C3, T1, and A1, for scaling the output voltage of the power amplifier means (Column 4, lines 15-27).

With respect to claims 56 and 57, Pollanen et al. disclose voltage scaling ratio controller means, element number A1, which as a result of its operation sets the voltage scaler means based upon a predetermined target output power of the amplifier means.

With respect to claim 58, Pollanen et al. disclose a current mirror means, combination of element numbers T1 and A2, for mirroring the output current wherein the output current is scaled using a predetermined current scaling ratio in A2 (Column 4, lines 28-37).

With respect to claim 59, Pollanen et al. disclose a linear multiplier means, M1, in figure 9.

With respect to claim 61, Pollanen et al. teach generating a control signal to vary the true output power delivered by the power amplifier means by the control line from element number 6 to element number 3 in figure 9 (Column 7, lines 39-52).

With respect to claims 65 and 66, Pollanen et al. disclose that the voltage detector means, current detector means, and power detector means are formed on a monolithic substrate (Column 3, lines 10-15).

With respect to claims 67 and 68, Pollanen et al. disclose the power amplifier comprises a power controller means, voltage detector means, current detector means, and power detector means (Column 3, lines 10-15).

With respect to claim 69, Pollanen et al. disclose the system comprises a transmitter portion means, element number 2, of a transceiver in figure 9 (Column 6, lines 34-39).

With respect to claim 71, Pollanen et al. disclose a method for controlling true output power of a transmitter in figure 9. Pollanen et al. disclose a voltage detector in communication with a power amplifier, which is in the transmitter element number 3, for detecting an output voltage, Vrf, of the power amplifier, which is proportional to the output voltage of the amplifier(Column 4, lines 14-27). Pollanen et al. also disclose a current detector that generates a current signal, Irf, that is proportional to the output current of the power amplifier (Column 4, lines 28-37). Pollanen et al. disclose a power detector in communication with the voltage detector and the current detector comprising a multiplier, element number M1, for multiplying the current signal and the voltage signal to generate a power signal, Pwdc, proportional to the true output power delivered by the power amplifier (Column 4, lines 38-47). Pollanen et al. further disclose a power controller, element number 6, in communication with the power detector and power amplifier for controlling the power amplifier to regulate the true output power delivered by the power amplifier based on the power signal (Column 7, lines 39-52 and Column 2, lines 36-42). Pollanen et al. further teach that the output voltage and output current of the power amplifier in element 3 are the output voltage and current of an output load, element number 4, of the transmitter ((Column 6, lines 40-41).

With respect to claim 72, Pollanen et al. disclose that the voltage signal and current signal, Vrf and Irf, must comprise a fundamental frequency component of the output voltage and current of the power amplifier since they are taken from the output stage of the amplifier (Column 4, lines 14-37). Pollanen et al. also disclose that eh power comprise a DC power signal, Pwdc (Column 4, lines 38-47).

With respect to claims 73-75, Pollanen et al. disclose a voltage scaler, comprising a capacitive voltage divider, element numbers C3, T1, and A1, for scaling the output voltage of the power amplifier (Column 4, lines 15-27).

With respect to claims 76 and 77, Pollanen et al. disclose voltage scaling ratio controller, element number A1, which as a result of its operation sets the voltage scaler based upon a predetermined target output power of the amplifier.

With respect to claim 78, Pollanen et al. disclose a current mirror, combination of element numbers T1 and A2, for mirroring the output current wherein the output current is scaled using a predetermined current scaling ratio in A2 (Column 4, lines 28-37).

With respect to claim 79, Pollanen et al. disclose a linear multiplier, M1, in figure 9.

With respect to claim 81, Pollanen et al. teach generating a control signal to vary the true output power delivered by the power amplifier by the control line from element number 6 to element number 3 in figure 9 (Column 7, lines 39-52).

With respect to claims 85 and 86, Pollanen et al. disclose that the power controller, power amplifier, voltage detector, current detector, and power detector are formed on a monolithic substrate (Column 3, lines 10-15).

With respect to claims 87 and 88, Pollanen et al. disclose the power amplifier comprises a power controller, voltage detector, current detector, and power detector (Column 3, lines 10-15).

With respect to claim 90, Pollanen et al. disclose a method for controlling true output power of a transmitter in figure 9. Pollanen et al. disclose monitoring an output

voltage of a power amplifier, which is in the transmitter element number 3, and producing a voltage signal, Vrf, which is proportional to the output voltage of the amplifier (Column 4, lines 14-27). Pollanen et al. disclose monitoring an output current of a power amplifier, which is in the transmitter element number 3, and producing a current signal, Irf, which is proportional to the output current of the amplifier (Column 4, lines 28-37). Pollanen et al. disclose multiplying with element number M1 the current signal and the voltage signal to generate a power signal, Pwdc, proportional to the true output power delivered by the power amplifier (Column 4, lines 38-47). Pollanen et al. further disclose controlling the power amplifier to regulate the true output power delivered by the power amplifier based on the power signal (Column 7, lines 39-52 and Column 2, lines 36-42). Pollanen et al. further teach that the output voltage and output current of the power amplifier in element 3 are the output voltage and current of an output load, element number 4, of the transmitter ((Column 6, lines 40-41).

With respect to claim 91, Pollanen et al. disclose that the voltage signal and current signal, Vrf and Irf, must comprise a fundamental frequency component of the output voltage and current of the power amplifier since they are taken from the output stage of the amplifier (Column 4, lines 14-37). Pollanen et al. also disclose that eh power comprise a DC power signal, Pwdc (Column 4, lines 38-47).

With respect to claims 92-94, Pollanen et al. disclose scaling the output voltage of the power amplifier with element numbers C3, T1, and A1, which as a result of its operation sets the voltage scaler based upon a predetermined target output power of the amplifier (Column 4, lines 15-27).

With respect to claim 95, Pollanen et al. disclose a current mirror, combination of element numbers T1 and A2, for mirroring the output current wherein the output current is scaled using a predetermined current scaling ratio in A2 (Column 4, lines 28-37).

With respect to claim 96, Pollanen et al. teach generating a control signal to vary the true output power delivered by the power amplifier by the control line from element number 6 to element number 3 in figure 9 (Column 7, lines 39-52).

With respect to claim 101, Pollanen et al. disclose a system for controlling true output power of a transmitter in figure 9. Pollanen et al. disclose means for monitoring an output voltage of a power amplifier, which is in the transmitter element number 3, and means for producing a voltage signal, Vrf, which is proportional to the output voltage of the amplifier (Column 4, lines 14-27). Pollanen et al. disclose means for monitoring an output current of a power amplifier, which is in the transmitter element number 3, and means for producing a current signal, Irf, which is proportional to the output current of the amplifier (Column 4, lines 28-37). Pollanen et al. disclose means for multiplying the current signal and the voltage signal to generate a power signal, Pwdc, proportional to the true output power delivered by the power amplifier (Column 4, lines 38-47). Pollanen et al. further disclose means for controlling the power amplifier to regulate the true output power delivered by the power amplifier based on the power signal (Column 7, lines 39-52 and Column 2, lines 36-42). Pollanen et al. further teach that the output voltage and output current of the power amplifier in element 3 are the output voltage and current of an output load, element number 4, of the transmitter (Column 6, lines 40-41).

With respect to claim 102, Pollanen et al. disclose that the voltage signal and current signal, Vrf and Irf, must comprise a fundamental frequency component of the output voltage and current of the power amplifier since they are taken from the output stage of the amplifier (Column 4, lines 14-37). Pollanen et al. also disclose that eh power comprise a DC power signal, Pwdc (Column 4, lines 38-47).

With respect to claims 103-105, Pollanen et al. disclose mean for scaling the output voltage of the power amplifier with element numbers C3, T1, and A1, which as a result of its operation sets the voltage scaler based upon a predetermined target output power of the amplifier (Column 4, lines 15-27).

With respect to claim 106, Pollanen et al. disclose a means for mirroring the current, combination of element numbers T1 and A2, for mirroring the output current wherein the output current is scaled using a predetermined current scaling ratio in A2 (Column 4, lines 28-37).

With respect to claim 107, Pollanen et al. teach means for generating a control signal to vary the true output power delivered by the power amplifier by the control line from element number 6 to element number 3 in figure 9 (Column 7, lines 39-52).

With respect to claims 111 and 112, Pollanen et al. disclose that the power controller, power amplifier, voltage detector, current detector, and power detector are formed on a monolithic substrate (Column 3, lines 10-15).

With respect to claims 113 and 114, Pollanen et al. disclose the power amplifier comprises a power controller, voltage detector, current detector, and power detector (Column 3, lines 10-15).

With respect to claim 115, Pollanen et al. disclose the system comprises a transmitter portion, element number 2, of a transceiver in figure 9 (Column 6, lines 34-39).

With respect to claim 117, Pollanen et al. disclose a computer program stored on a tangible computer medium for controlling true output power of a transmitter in figure 9. Pollanen et al. disclose monitoring an output voltage of a power amplifier, which is in the transmitter element number 3, and producing a voltage signal, Vrf, which is proportional to the output voltage of the amplifier (Column 4, lines 14-27). Pollanen et al. disclose monitoring an output current of a power amplifier, which is in the transmitter element number 3, and producing a current signal, Irf, which is proportional to the output current of the amplifier (Column 4, lines 28-37). Pollanen et al. disclose multiplying with element number M1 the current signal and the voltage signal to generate a power signal, Pwdc, proportional to the true output power delivered by the power amplifier (Column 4, lines 38-47). Pollanen et al. further disclose controlling the power amplifier to regulate the true output power delivered by the power amplifier based on the power signal (Column 7, lines 39-52 and Column 2, lines 36-42). Pollanen et al. further teach that the output voltage and output current of the power amplifier in element 3 are the output voltage and current of an output load, element number 4, of the transmitter ((Column 6, lines 40-41).

With respect to claim 118, Pollanen et al. disclose that the voltage signal and current signal, Vrf and Irf, must comprise a fundamental frequency component of the output voltage and current of the power amplifier since they are taken from the output

stage of the amplifier (Column 4, lines 14-37). Pollanen et al. also disclose that eh power comprise a DC power signal, Pwdc (Column 4, lines 38-47).

With respect to claims 119-120, Pollanen et al. disclose scaling the output voltage of the power amplifier with element numbers C3, T1, and A1, which as a result of its operation sets the voltage scaler based upon a predetermined target output power of the amplifier (Column 4, lines 15-27).

With respect to claim 121, Pollanen et al. disclose a current mirror, combination of element numbers T1 and A2, for mirroring the output current wherein the output current is scaled using a predetermined current scaling ratio in A2 (Column 4, lines 28-37).

With respect to claim 122, Pollanen et al. teach generating a control signal to vary the true output power delivered by the power amplifier by the control line from element number 6 to element number 3 in figure 9 (Column 7, lines 39-52).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 42-44, 62-64, 82-84, 97-99, 108-110, and 123-125 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pollanen et al. (U.S. 6,289,205) in view of McGirr et al. (U.S. 5,129,098).

With respect to claim 42, the system of Pollanen et al. is described above in the discussion of claims 31 and 41. Pollanen et al. do not expressly disclose a comparator in the power controller. However, McGirr et al. disclose a power controller for an amplifier according to a measured power signal in figure 4 thus making it analogous art since it is in the same field of endeavor. McGirr et al. teach using a comparator, element number 108, for comparing the power signal with at least one predetermined threshold and generating a control signal based upon that comparison (Column 6, lines 7-28). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to apply the comparator technique of McGirr et al. in the system of Pollanen et al. in order to control the gain of the amplifier based upon target values.

With respect to claim 43, McGirr et al. further disclose two predetermined thresholds wherein the first predetermined threshold is greater than the second threshold and using the control signal to cause the output power of the power amplifier to decrease when the power signal exceeds the first predetermined threshold and increase when the power signal is less than the second predetermined threshold (Column 7, lines 40-56). Therefore, it would be obvious to one of ordinary skill in the are at the time of the applicant's invention to apply the two threshold comparator

technique of McGirr et al. in the system of Pollanen et al. in order to keep the gain of the amplifier in a prescribed range.

With respect to claim 44, McGirr et al. further disclose using the control signal to cause the output power of the power amplifier to decrease when the power signal exceeds the first predetermined threshold and increase when the power signal is less than the threshold (Column 6, lines 7-28). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to apply the comparator technique of McGirr et al. in the system of Pollanen et al. in order to control the gain of the amplifier based upon target values.

With respect to claim 62, the system of Pollanen et al. is described above in the discussion of claims 51 and 61. Pollanen et al. do not expressly disclose a comparator means in the power controller. However, McGirr et al. disclose a power controller means for an amplifier means according to a measured power signal in figure 4 thus making it analogous art since it is in the same field of endeavor. McGirr et al. teach using a comparator means, element number 108, for comparing the power signal with at least one predetermined threshold and generating a control signal based upon that comparison (Column 6, lines 7-28). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to apply the comparator means technique of McGirr et al. in the system of Pollanen et al. in order to control the gain of the amplifier based upon target values.

With respect to claim 63, McGirr et al. further disclose two predetermined thresholds wherein the first predetermined threshold is greater than the second

threshold and using the control signal to cause the output power of the power amplifier means to decrease when the power signal exceeds the first predetermined threshold and increase when the power signal is less than the second predetermined threshold (Column 7, lines 40-56). Therefore, it would be obvious to one of ordinary skill in the are at the time of the applicant's invention to apply the two threshold comparator technique of McGirr et al. in the system of Pollanen et al. in order to keep the gain of the amplifier in a prescribed range.

With respect to claim 64, McGirr et al. further disclose using the control signal to cause the output power of the power amplifier to decrease when the power signal exceeds the first predetermined threshold and increase when the power signal is less than the threshold (Column 6, lines 7-28). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to apply the comparator technique of McGirr et al. in the system of Pollanen et al. in order to control the gain of the amplifier based upon target values.

With respect to claim 82, the method of Pollanen et al. is described above in the discussion of claims 71 and 81. Pollanen et al. do not expressly disclose a comparator in the power controller. However, McGirr et al. disclose a power controller for an amplifier according to a measured power signal in figure 4 thus making it analogous art since it is in the same field of endeavor. McGirr et al. teach using a comparator, element number 108, for comparing the power signal with at least one predetermined threshold and generating a control signal based upon that comparison (Column 6, lines 7-28). Therefore, it would be obvious to one of ordinary skill in the art at the time of the

applicant's invention to apply the comparator technique of McGirr et al. in the method of Pollanen et al. in order to control the gain of the amplifier based upon target values.

With respect to claim 83, McGirr et al. further disclose two predetermined thresholds wherein the first predetermined threshold is greater than the second threshold and using the control signal to cause the output power of the power amplifier to decrease when the power signal exceeds the first predetermined threshold and increase when the power signal is less than the second predetermined threshold (Column 7, lines 40-56). Therefore, it would be obvious to one of ordinary skill in the are at the time of the applicant's invention to apply the two threshold comparator technique of McGirr et al. in the method of Pollanen et al. in order to keep the gain of the amplifier in a prescribed range.

With respect to claim 84, McGirr et al. further disclose using the control signal to cause the output power of the power amplifier to decrease when the power signal exceeds the first predetermined threshold and increase when the power signal is less than the threshold (Column 6, lines 7-28). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to apply the comparator technique of McGirr et al. in the method of Pollanen et al. in order to control the gain of the amplifier based upon target values.

With respect to claim 97, the method of Pollanen et al. is described above in the discussion of claims 90 and 96. Pollanen et al. do not expressly disclose a comparator in the power controller. However, McGirr et al. disclose a power controller for an amplifier according to a measured power signal in figure 4 thus making it analogous art

since it is in the same field of endeavor. McGirr et al. teach using a comparator, element number 108, for comparing the power signal with at least one predetermined threshold and generating a control signal based upon that comparison (Column 6, lines 7-28). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to apply the comparator technique of McGirr et al. in the method of Pollanen et al. in order to control the gain of the amplifier based upon target values.

With respect to claim 98, McGirr et al. further disclose two predetermined thresholds wherein the first predetermined threshold is greater than the second threshold and using the control signal to cause the output power of the power amplifier to decrease when the power signal exceeds the first predetermined threshold and increase when the power signal is less than the second predetermined threshold (Column 7, lines 40-56). Therefore, it would be obvious to one of ordinary skill in the are at the time of the applicant's invention to apply the two threshold comparator technique of McGirr et al. in the method of Pollanen et al. in order to keep the gain of the amplifier in a prescribed range.

With respect to claim 99, McGirr et al. further disclose using the control signal to cause the output power of the power amplifier to decrease when the power signal exceeds the first predetermined threshold and increase when the power signal is less than the threshold (Column 6, lines 7-28). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to apply the comparator technique of McGirr et al. in the method of Pollanen et al. in order to control the gain of the amplifier based upon target values.

With respect to claim 108, the system of Pollanen et al. is described above in the discussion of claims 101 and 107. Pollanen et al. do not expressly disclose a comparator in the power controller. However, McGirr et al. disclose a power controller for an amplifier according to a measured power signal in figure 4 thus making it analogous art since it is in the same field of endeavor. McGirr et al. teach using a comparator, element number 108, for comparing the power signal with at least one predetermined threshold and generating a control signal based upon that comparison (Column 6, lines 7-28). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to apply the comparator technique of McGirr et al. in the system of Pollanen et al. in order to control the gain of the amplifier based upon target values.

With respect to claim 109, McGirr et al. further disclose two predetermined thresholds wherein the first predetermined threshold is greater than the second threshold and using the control signal to cause the output power of the power amplifier to decrease when the power signal exceeds the first predetermined threshold and increase when the power signal is less than the second predetermined threshold (Column 7, lines 40-56). Therefore, it would be obvious to one of ordinary skill in the are at the time of the applicant's invention to apply the two threshold comparator technique of McGirr et al. in the system of Pollanen et al. in order to keep the gain of the amplifier in a prescribed range.

With respect to claim 110, McGirr et al. further disclose using the control signal to cause the output power of the power amplifier to decrease when the power signal

exceeds the first predetermined threshold and increase when the power signal is less than the threshold (Column 6, lines 7-28). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to apply the comparator technique of McGirr et al. in the system of Pollanen et al. in order to control the gain of the amplifier based upon target values.

With respect to claim 123, the "computer program" of Pollanen et al. is described above in the discussion of claims 117 and 122. Pollanen et al. do not expressly disclose a comparator in the power controller. However, McGirr et al. disclose a power controller for an amplifier according to a measured power signal in figure 4 thus making it analogous art since it is in the same field of endeavor. McGirr et al. teach using a comparator, element number 108, for comparing the power signal with at least one predetermined threshold and generating a control signal based upon that comparison (Column 6, lines 7-28). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to apply the comparator technique of McGirr et al. in the "computer program" of Pollanen et al. in order to control the gain of the amplifier based upon target values.

With respect to claim 124, McGirr et al. further disclose two predetermined thresholds wherein the first predetermined threshold is greater than the second threshold and using the control signal to cause the output power of the power amplifier to decrease when the power signal exceeds the first predetermined threshold and increase when the power signal is less than the second predetermined threshold (Column 7, lines 40-56). Therefore, it would be obvious to one of ordinary skill in the art

at the time of the applicant's invention to apply the two threshold comparator technique of McGirr et al. in the "computer program" of Pollanen et al. in order to keep the gain of the amplifier in a prescribed range.

With respect to claim 125, McGirr et al. further disclose using the control signal to cause the output power of the power amplifier to decrease when the power signal exceeds the first predetermined threshold and increase when the power signal is less than the threshold (Column 6, lines 7-28). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to apply the comparator technique of McGirr et al. in the "computer program" of Pollanen et al. in order to control the gain of the amplifier based upon target values.

7. Claims 40, 60, and 80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pollanen et al. (U.S. 6,289,205) in view of Summers et al. (U.S. 2004/0266371).

With respect to claim 40, the system of Pollanen et al. is described above in the discussion of claims 31 and 39. Pollanen et al. do not disclose a Gilbert-cell multiplier. However, Summers et al. disclose power control technique of a transmitting power amplifier thus making it analogous art since it is in the same field of endeavor. Summers et al. teach using a Gilbert-cell multiplier for multiplying the measured values and getting a power value (Paragraph 39). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to use a Gilbert-cell

multiplier as taught by Summers et al. in the system of Pollanen et al. in order to use a multiplier, which is well known in the art.

With respect to claim 60, the system of Pollanen et al. is described above in the discussion of claims 51 and 59. Pollanen et al. do not disclose a Gilbert-cell multiplier means. However, Summers et al. disclose power control technique of a transmitting power amplifier thus making it analogous art since it is in the same field of endeavor. Summers et al. teach using a Gilbert-cell multiplier means for multiplying the measured values and getting a power value (Paragraph 39). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to use a Gilbert-cell multiplier means as taught by Summers et al. in the system of Pollanen et al. in order to use a multiplier, which is well known in the art.

With respect to claim 80, the method of Pollanen et al. is described above in the discussion of claims 71 and 79. Pollanen et al. do not disclose a Gilbert-cell multiplier. However, Summers et al. disclose power control technique of a transmitting power amplifier thus making it analogous art since it is in the same field of endeavor. Summers et al. teach using a Gilbert-cell multiplier for multiplying the measured values and getting a power value (Paragraph 39). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to use a Gilbert-cell multiplier as taught by Summers et al. in the method of Pollanen et al. in order to use a multiplier, which is well known in the art.

8. Claims 50, 70, 89, 100, and 116 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pollanen et al. (U.S. 6,289,205).

With respect to claim 50, the system of Pollanen et al. is described above in the discussion of claim 31. Pollanen et al. do not specifically disclose using 802.11 standards. However, 802.11 standards are extremely well known in the art. Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to be compliant with 802.11 standards in order to be compatible with this format since it is widely used.

With respect to claim 70, the system of Pollanen et al. is described above in the discussion of claim 51. Pollanen et al. do not specifically disclose using 802.11 standards. However, 802.11 standards are extremely well known in the art. Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to be compliant with 802.11 standards in order to be compatible with this format since it is widely used.

With respect to claim 89, the method of Pollanen et al. is described above in the discussion of claim 71. Pollanen et al. do not specifically disclose using 802.11 standards. However, 802.11 standards are extremely well known in the art. Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to be compliant with 802.11 standards in order to be compatible with this format since it is widely used.

With respect to claim 100, the method of Pollanen et al. is described above in the discussion of claim 90. Pollanen et al. do not specifically disclose using 802.11 standards. However, 802.11 standards are extremely well known in the art. Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to be compliant with 802.11 standards in order to be compatible with this format since it is widely used.

With respect to claim 116, the system of Pollanen et al. is described above in the discussion of claim 101. Pollanen et al. do not specifically disclose using 802.11 standards. However, 802.11 standards are extremely well known in the art. Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to be compliant with 802.11 standards in order to be compatible with this format since it is widely used.

Allowable Subject Matter

9. Claims 1-30 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adeel Haroon whose telephone number is (571) 272-

7405. The examiner can normally be reached on Monday thru Friday, 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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